PENDING CLAIMS

The following is a detailed listing of all pending claims of the Application.

1. (Original) An electromagnetic interference cancellation system comprising

a control signal generation unit having a counter that counts n-bit signals to output a first output signal of n bits with a count value, and a second output signal having a level that is opposite to the first output signal, the control signal generation unit alternately outputs the first and second output signals as control signals according to a cycle of the counter;

a voltage control unit that outputs a voltage having a step index level corresponding to the count value of the control signal; and

an oscillator that generates a clock signal having a frequency corresponding to the voltage outputted from the voltage control unit.

2. (Original) The system of claim 1, wherein the counter comprises n first flip-flops that output 1 bit of the first and second output signals respectively, the flip-flops being coupled to each other in series, and

the first flip-flop is triggered to reverse an output at an edge where a first output signal of a previous first flip-flop becomes a first level.

3. (Original) The system of claim 2, wherein the control signal generation unit comprises:

a second flip-flop coupled to a final first flip-flop of the counter in series so as to reverse an output at an edge where a first output signal of the final first flip-flop becomes the first level; and

a multiplexer that alternately outputs the first and second output signals of the n first flip-flops whenever the output level of the second flip-flop is reversed.

4. (Original) The system of claim 3, wherein the multiplexer comprises a first transmission gate for passing the first output signal when the first and second output signals of the first flip-flop are inputted and the output of the second flip-flop is a high level, and a second transmission gate for passing the second output signal when the output of the second flip-flop is a low level.

5. (Original) The system of claim 1, wherein the voltage control unit generates step index voltage having 2n voltage levels corresponding to the count values, and the step index voltage increases and decreases according to the cycle of the counter.

6. (Original) The system of claim 1, wherein the oscillator receives the voltage of the voltage control unit as a high level voltage, and generates a clock signal having a frequency which is in inverse proportion to a difference between the high level voltage and a reference low level voltage.

7. (Original) An EMI cancellation system comprising:

a control signal generation unit comprising a counter having n first flip-flops that respectively output first and second output signals with opposite levels, the n first flip-flops being coupled to each other in series and each first flip-flop reversing outputs at every cycle of the first and second signals of a previous first flip-flop, a second flip-flop that outputs third and fourth output signals having opposite levels and being reversed at every cycle of the first and second output signals of a final first flip-flop of the counter, and a multiplexer for passing the first signals of the n first flip-flops as a control signal of n bits when the third output signal of the second flip-flop is a first level and passing the second output signals of the n first flip-flops as the control signal of n bits when the third output signal of the second flip-flop is a second level;

a voltage control unit that outputs voltages having respective step index levels corresponding to count values of n-bit control signals; and

an oscillator that generates a clock signal having a frequency corresponding to the step index level of the voltage of the voltage control unit.

8. (Original) A method for canceling electromagnetic interference by generating clock signals having various frequencies in a predetermined range, the method comprising:

alternately outputting an n-bit signal and a reverse signal of the n-bit signal at every cycle of the counter, the n-bit signal being counted by an n-bit counter;

generating an output voltage having a step index level which increases or decreases stepwise according to a count value of the control signal; and

generating a clock signal having a frequency corresponding to the level of the output voltage.

9. (Original) The method of claim 8, wherein the step index level of the output voltage alternately increases and decreases according to the cycle of the counter.

10. (Original) The method of claim 8, wherein the clock signal is generated by an oscillator which receives the output voltage as a high level voltage such that the clock signal has a pulse width proportional to a difference between the high level voltage and a reference low level voltage.